rejections). No new matter has been added. Claims 1-7 are presented for reconsideration.

35 U.S.C. § 103(a)

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yamamoto (JP410144938A) in view of Kobayashi (U.S. Patent No. 5,973,359). In making this rejection, the Office Action asserts that the combination of these two references teaches and/or suggests each and every element of the claimed invention. The Office Action also asserts that it would be obvious to one of ordinary skill in the art to combine these two references. Applicants respectfully request reconsideration of this rejection.

Claim 1 recites a semiconductor device. This device includes an insulating gate field effect transistor. This transistor includes a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel. A protective diode is connected between a gate and a source of the insulating gate field effect transistor to break down an input of a constant voltage or more applied between the gate and the source. The protective diode is formed as a bidirectional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers are flatly and alternately provided on an insulating layer at a peripheral portion than the transistor cells. Metal films in a ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively. Each of the metal films is successively formed with either a source wiring or a gate electrode pad consisting of a metal film, respectively.

The present invention improves the function of the protective diode by lowering the serial resistance of the protective diodes connected between a gate and a source of an insulating gate field effect transistor. As discussed above, this invention includes (1) a protective diode that is mounted on the chip outer circumference (peripheral portion of a chip) to increase the area of the p-n junction, and (2) connections between the source electrode and the gate electrode on both end portions of the protective diode are brought in contact not with a semiconductor diffusion area or polysilicon film but with a ring-form metal film provided along the full circumferential length of the diode. An illustrative example of this configuration is provided in Figure 1(b) of the present specification. In Figure 1(b), reference numeral 1 references the protective diode and reference numerals 2 and 3 represent the metal films.

Yamamoto teaches item (1) above. Specifically, Yamamoto discloses a protective diode that is mounted on the chip outer circumference (peripheral portion of a chip) to increase the area of the p-n junction. Yamamoto also discloses a source electrode 16 that is mounted on the top surface of the semiconductor device. Yamamoto, however, fails to teach and/or suggest using a metallic film around the outermost circumference of the protective diode as recited in claim 1.

The outermost circumference of Yamamoto is assumed to be connected by the generally practiced method used in this type of semiconductor device. Specifically, the outermost circumference of the protective diode is connected to the gate electrodes by forming a gate pad in such a manner as to be connected at one part of the outermost circumference. Polysilicon film, however, provides greater resistance than a metal film. The use of the polysilicon film increases the resistance of the protective diode.

Accordingly, the entire circumferential length does not function as a low resistance diode, because the remote portion from the part connected to the gate pad has the added resistance of the circumferential length of polysilicon. Accordingly, the serial resistance increases. Accordingly, Yamamoto fails to disclose and/or suggest metal films in ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers, respectively.

The Office Action admits that Yamamoto does not teach that the transistor is formed from a plurality of transistor cells. The Office Action cites Kobayashi as correcting this deficiency in Yamamoto.

While Kobayashi may disclose a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel, Kobayashi fails to correct the deficiencies discussed above in Yamamoto. Specifically, Kobayashi fails to show metal films in ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively.

Accordingly, the combination of Yamamoto and Kobayashi fails to teach and/or suggest the claimed invention. Specifically, the combination of these references fails to disclose and/or suggest metal films in ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection of claim 1 under 35 U.S.C. § 103(a).

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Williams (U.S. Patent No. 6,268,242) and Yamamoto (discussed above). Applicants request reconsideration of this rejection.

Williams discloses forming a diode around the gate pad described in Figure 9 of the present application. In this construction, the gate pad is connected directly to the inner circumferential edge of the diode. The outer circumferential end of the diode is connected to the source wiring that is connected to the transistor cells located around the diode.

The Office Action admits that Williams does not teach that the metal film contacting the innermost and outermost layers is ring-shaped. The Office Action, however, asserts that it would have been obvious to improve the invention of Williams to include such ring-shaped contacts in view of Yamamoto, since Yamamoto teaches forming the Zener diode in a ring-shape for the purpose of increasing the electrostatic strength of the Zener diode.

Williams, however, does not disclose that connecting both end portions of the diode with metal films reinforces the protective functions of the diode. Additionally, if the diode of Williams is formed into a ring form and positioned on the periphery of the integrated circuit, there would be no cell area around the outer circumference to form a cell area. Accordingly, it would not be obvious to one of ordinary skill in the art to convert the diode construction taught in Williams into a ring form.

In contrast, Yamamoto discloses increasing the protective function of the diode by increasing the area of the p-n junction. Yamamoto, however, does not teach and or suggest connecting the outermost layer of the diode with metal film for further lowering the serial resistance while providing a diode on the chip outer circumference.

Since Williams fails to teach and/or suggest that the protective function of the diode could be improved by use of metal films to connect both end portions of the diode,

it would not be obvious to combine Williams and Yamamoto since the conversion of the Zener diode shown in Williams to the ring-shaped Zener diode shown in Yamamoto would require the displacement of the transistor cells taught in Yamamoto. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-6 under 35 U.S.C. § 103(a).

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams and Yamamoto (discussed above) or over Yamamoto and Kobayashi (both discussed above) as applied to claim 1 above, and further in view of Throngnumchai (US. Patent No. 4,963,970).

With respect to claim 7, the present invention forms a bidirectional diode in the longitudinal direction using a lamination of three or more layers. The bottom layer and the top layer are brought into contact with the metal films. Throngnumchai, however, only discloses a two-layer construction. Accordingly, this reference fails to teach and/or suggest the invention recited in claim 7. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 7 under 35 U.S.C. § 103(a).

Claim Amendments

Applicants have amended claims 6 and 7. The amendments to claim 6 improve the readability and clarity of this claim.

Claim 7 has been amended to place this claim in independent form. Accordingly, the amendments to claim 7 are clerical in nature and are not intended to limit the scope of this claim.

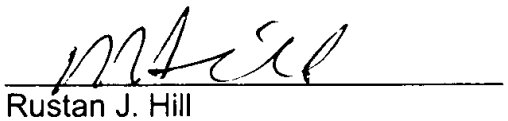
Conclusion

Applicants' remarks have overcome the rejection set forth in the Office Action dated October 24, 2002. Specifically, Applicants' remarks have distinguished claim 1 from the combination of Yamamoto and Kobayashi and thus overcome the rejection of this claim under 35 U.S.C. § 103(a). Applicants' remarks have also distinguished claims 1-6 from the combination of Williams and Yamamoto and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have also distinguished claim 7 from the combination of Williams, Yamamoto and Throngnumchai or the combination of Yamamoto, Kobayashi and Throngnumchai and thus overcome the rejection of this claim under 35 U.S.C. § 103(a). Accordingly, claims 1-7 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-7.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 107400-00044.

Respectfully submitted,



Rustan J. Hill
Registration No. 37,351

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

RJH/elz

Enclosures: Marked-Up Copy of Amended Claims
Petition for Extension of Time

MARKED-UP COPY OF AMENDED CLAIMS

6. (Twice Amended) The semiconductor device of claim 1, wherein a diffusion region having a [difference] different conductivity type from that of said semiconductor layer is formed on the closest side to said protective diode of said transistor cells arranged, said diffusion region having no other diffusion region therein, and said source wiring contacted to the most inner layer of said protective diode is contacted to said diffusion region.

7. (Amended) A semiconductor device [according to claim 1, wherein said p-type layers and said n-type layers comprising said bidirectional diode are not flatly formed but are alternately formed in a height direction] comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel; and

a protective diode connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and said source,

wherein said protective diode is formed as a bidirectional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers are alternately laminated in a height direction three or more layers on an insulating layer at a peripheral portion of said transistor cells, ring-shaped metal films contacting with the bottom layer and the top layer of said p-type layers or said n-type layers are formed respectively, and each of said metal films is successively formed with either of a source wiring or a gate electrode pad consisting of a metal film, respectively.

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